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Noise in metallic set transistors of the different contact area between their islands and a substrate

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The problem of background charge fluctuations in Single Electron Tunneling (SET) circuits is put in the forefront in recent investigations of SET devices. At low frequencies, these fluctuations substantially dominate over intrinsic fluctuations in SET devices and are usually characterized by a $1/f$ spectrum with a roll-off frequency of $0.1 \div 1$ kHz and intensity of $10^{-4} \div 10^{-3} e/\sqrt{\text{Hz}}$ at 10 Hz (see, for example, [1] and refs. therein). Such fluctuations can dramatically depress the performance of SET devices. For instance, they superimpose the limitation on sensitivity of an SET transistor used as an electrometer [2].

Although the intensity of background charge noise depends on many factors and widely varies from sample to sample, it was noticed a trend of its increase with the island size [3]. This might be qualitatively explained by the important role the substrate plays as a source of charge fluctuations. In particular, recent measurements using Al-based SET electrometers of stacked design [4] showed that the noise level can be decreased down to the value of $2.5 \cdot 10^{-5} e/\sqrt{\text{Hz}}$ at 10 Hz.

The aim of this work was to systematically examine SET transistors with different contacting areas between transistor islands and the substrate (keeping their electric parameters nominally similar). These areas varied from 50% to almost zero of the total island area (Fig. 1). The transistor 4 (Fig. 1) was practically insensitive to charge noise sources located in a substrate. Four chips (A-D), each comprising a series of four transistors (1-4), have been fabricated and studied.

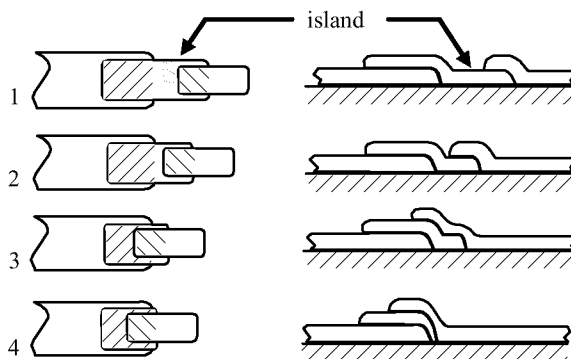


Fig 1. Four transistor structures with different island/substrate contact area.

The Al film structures (Fig. 2) with Al/AIO_x/Al tunnel junctions were fabricated on a Si substrate buffered by sputtered Al₂O₃ layer 200 nm thick. The e-beam lithography

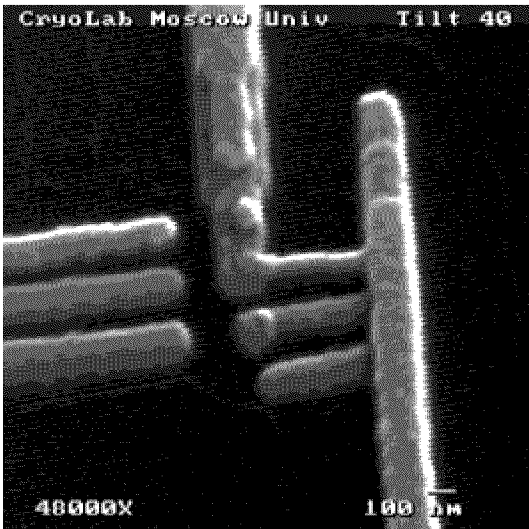


Fig 2. SEM image of the experimental structure.

Table 1. Noise level vs the island/substrate contact area for transistors on chip B at $I = 50$ pA.

transistor number	1	2	3	4
Nominal contact area of an island to the substrate (% of total island area)	50	40	20	0
Charge noise at 10 Hz, $10^{-5}e/\sqrt{Hz}$	25	14	11	7

and traditional shadow evaporation technique were used for the fabrication process. There were three successive deposition cycles in-situ with different angles and two oxidation processes in between. The characteristics of the sample were measured in a dilution refrigerator at the bath temperature $T = 25$ mK. The samples were voltage biased and the current I was measured. The noise floor of the setup was of the order of $20 \text{ fA}/\sqrt{Hz}$ at 10 Hz. SEM image of the experimental structure.

In all measured samples the noise level showed strong dependence on the contact area between the island and the substrate: the transistors with smaller contact area produce definitely less noise (see Table 1). At lower values of transport current I the equivalent charge noise of the transistors, which had no contact with the substrate (configuration 4 in Fig. 1), turned out to be suprisingly low for all the samples (see Table 2).

Table 2. The noise level of the samples of stacked design (transistor 4 in Fig. 1) at $I = 20 \div 30$ pA.

chip	A	B	C	D
Charge noise at 10 Hz, $10^{-5}e/\sqrt{Hz}$	2.5	4	7	5
Energy sensitivity	230	500	1200	800

However, the measured noise levels are still higher than the fundamental noise floor, determined by shot noise [2] (and evaluated for our transistors as $3 \cdot 10^{-6} e / \sqrt{Hz}$). Thus, we attribute the observed noise to fluctuations of both the background charges inside the tunnel barriers and tunnel conductances [5]. The latter manifest themselves in an anomalous noise dependence on a polarization charge on the island.

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